FEATURES

- Fully compatible with the ISO 11898 standard
- AEC-Q100 qualified
- Thermally protected
- Overcurrent protection function
- Transmit Data (TXD) dominant time-out function
- Silent mode in which the transmitter is disabled
- Transceiver in unpowered state disengages from the bus (zero load)
- At least 110 nodes can be connected
- High speed (up to 1 MBaud)
- Very low Electro Magnetic Emission (EME)
- Available in leadless DFN3*3-8 package, with small shape.

PRODUCT APPEARANCE

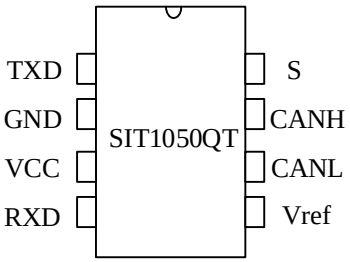
Provide green and environmentally friendly lead-free package

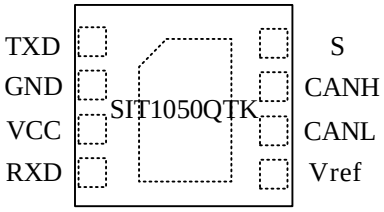
DESCRIPTION

The SIT1050Q is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. It is primarily intended for high-speed applications, up to 1 MBaud, in in-vehicle. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Supply voltage	V_{cc}		4.75	5.25	V
Maximum transmission rate	$1/t_{bit}$	Non-return to zero code	1		Mbaud
DC voltage at pin CANH and CANL	V_{can}		-40	+40	V
Bus differential voltage	V_{diff}		1.5	3.0	V
Virtual junction temperature	T_j		-40	150	℃
ESD capability	V_{esd}	HBM	±8		kV

PIN CONFIGURATION



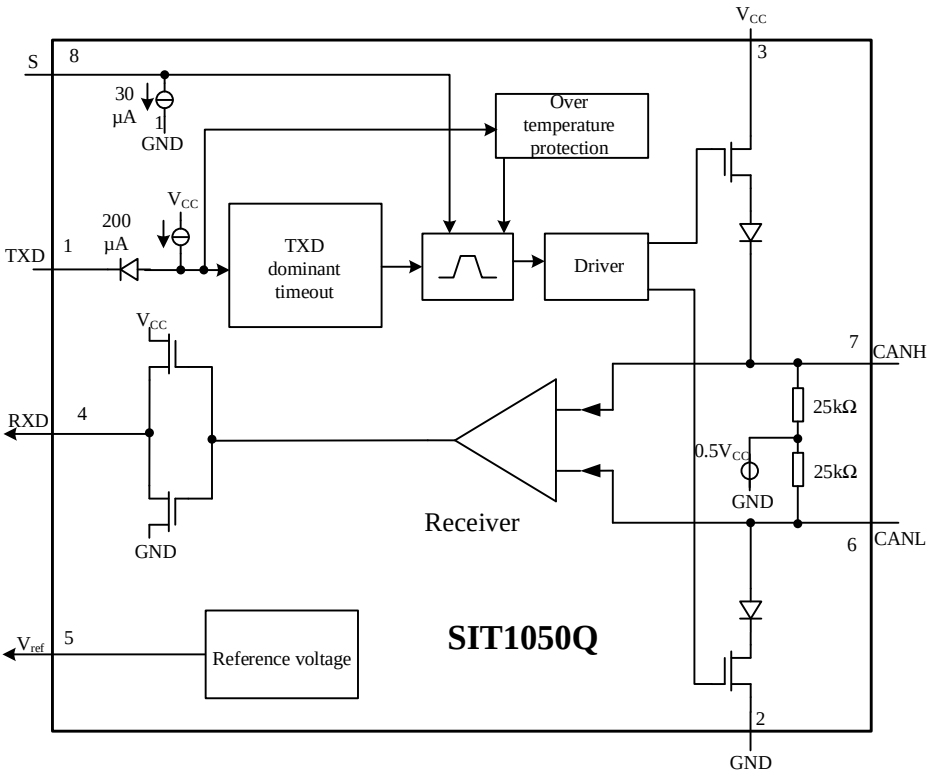


PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	TXD	transmit data input
2	GND	ground supply
3	VCC	supply voltage
4	RXD	receive data output; reads out data from the bus lines
5	Vref	reference voltage output
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	S	silent mode control input

NOTE: The exposed center pad of the DFN3*3-8 package is internal connected to the GND PIN of the chip. For enhanced thermal performance, the exposed center pad of the DFN3*3-8 package could be soldered to board ground.

INTERNAL BLOCK DIAGRAM



SIT1050Q internal block diagram

LIMITING VALUES

PARAMETER	SYMBOL	VALUE	UNIT
Supply voltage	V_{CC}	-0.3~+6	V
DC voltage on TXD/RXD/S/Vref pins	TXD, RXD, Vref, S	-0.3~VCC+0.3	V
Voltage range at any bus terminal (CANH, CANL)	CANL, CANH	-40~40	V
Storage temperature	T_{stg}	-55~150	℃
Ambient temperature	T_{amb}	-40~125	℃
Virtual junction temperature	T_j	-40~150	℃
Welding temperature range		300	℃

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

DRIVER ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
CANH dominant output voltage	$V_{OH(D)}$	VI=0V, S=0V, RL=60Ω, Fig.1, Fig.2	2.75	3.5	4.5	V
CANL dominant output voltage	$V_{OL(D)}$		0.5	1.5	2.25	V
Bus recessive output voltage	$V_{O(R)}$	VI=3V, S=0V, RL=60Ω, Fig.1, Fig.2	2	2.5	3	V
Bus dominant differential output voltage	$V_{OD(D)}$	VI=0V, S=0V, RL=60Ω, Fig.1, Fig.2	1.5		3	V
Bus recessive differential output voltage	$V_{OD(R)}$	VI=3V, S=0V, Fig.1, Fig.2	-0.012		0.012	V
		VI=3V, S=0V, NO LOAD	-0. 5		0.05	V
Transmitter voltage symmetry	V_{TXsym}	$V_{TXsym}=V_{CANH}+V_{CANL}$	$0.9V_{CC}$		$1.1V_{CC}$	V
Common-mode output voltage	V_{OC}	S=0V, Fig.8	2	2.5	3	V
Peak-to-peak Common-mode output voltage	$\triangle V_{OC}$			30		mV
Short-circuit output current	I_{OS}	CANH=-12V, CANL=open, Fig.11	-105	-40		mA
		CANH=12V, CANL=open, Fig.11		0.36	1	mA
		CANL=-12V, CANH=open, Fig.11	-1	0.5		mA
		CANL=12V, CANH=open, Fig.11		40	105	mA
Recessive output current	$I_{O(R)}$	-27V<CANH<32V 0<VCC<5.25V	-2.0		2.5	mA

(Unless specified otherwise; V_{CC}=5V±5% and -40°C≤T_j≤150°C, typical in V_{CC}=+5V and T_{amb}=25°C).

DRIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high-level output	t_{PLH}	S=0V, Fig.4	25	65	120	ns
Propagation delay time, high-to-low-level output	t_{PHL}		20	45	90	ns

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Differential output signal rise time	t_r			25		ns
Differential output signal fall time	t_f			50		ns
Enable time from silent mode to dominant	t_{EN}	Fig.7			1	μs
Bus dominant time-out time	t_{dom}	Fig.10	300	450	700	μs

(Unless specified otherwise; V_{CC}=5V±5% and -40°C≤T_j≤150°C, typical in V_{CC}=+5V and T_{amb}=25°C).

RECEIVER ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Positive-going input threshold voltage	V_{IT+}	S=0V, Fig.5		750	900	mV
Negative-going input threshold voltage	V_{IT-}		500	650		mV
Hysteresis voltage ($V_{IT+} - V_{IT-}$)	V_{HYS}		80	100		mV
High-level output voltage	V_{OH}	IO=-2mA, Fig.6	4	4.6		V
Low-level output voltage	V_{OL}	IO=2mA, Fig.6		0.2	0.4	V
Power-off bus input current	$I_{(OFF)}$	CANH or CANL=5V, Other pin=0V		3	20	μA
Input capacitance to ground, (CANH or CANL)	C_I			13		pF
Differential input capacitance	C_{ID}			5		pF
Input resistance, (CANH or CANL)	R_{IN}	TXD=3V, STB=0V	15	30	45	kΩ
Differential input resistance	R_{ID}		30		80	kΩ
Input resistance matching	RI_{match}	CANH=CANL	-3%		3%	
The range of common-mode voltage	V_{COM}		-12		12	V

(Unless specified otherwise; V_{CC}=5V±5% and-40°C≤T_j≤150°C, typical in V_{CC}=+5V and T_{amb}=25°C).

RECEIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high-level output	t_{PLH}	S=0V or VCC, Fig.6	60	100	130	ns
Propagation delay time, high-to-low-level output	t_{PHL}		45	70	100	ns
RXD signal rise time	tr			8		ns
RXD signal fall time	tf			8		ns

(Unless specified otherwise; V_{CC}=5V±5% and -40°C≤T_j≤150°C, typical in V_{CC}=+5V and T_{amb}=25°C)

DEVICE SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Loop delay1, driver input to receiver output, Recessive to Dominant	$t_{d(LOOP1)}$	S=0V, Fig.9	90		190	ns
Loop delay 2, driver input to receiver output, Dominant to Recessive	$t_{d(LOOP2)}$		90		190	ns

(Unless specified otherwise; V_{CC}=5V±5% and -40°C≤T_j≤150°C, typical in V_{CC}=+5V and T_{amb}=25°C).

OVER TEMPERATURE PROTECTION

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Shutdown junction temperature	$T_{j(sd)}$			160		℃

TXD-PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	I_{IH}(TXD)	VI=VCC	-2		2	μA
LOW-level input current	I_{IL}(TXD)	VI=0	-50		-10	μA
When VCC=0V, current on TXD pin	I_O(off)	VCC=0V, TXD=5V			1	μA
HIGH-level input voltage	V_{IH}		2		VCC+0.3	V
LOW-level input voltage	V_{IL}		-0.3		0.8	V

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Open voltage on TXD pin	TXD_O		H			logic

(Unless specified otherwise; V_{CC}=5V±5% and -40°C≤T_j≤150°C, typical in V_{CC}=+5V and T_{amb}=25°C).

STB PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input voltage	V_{IH}		2.0		VCC+0.3	V
LOW-level input voltage	V_{IL}		-0.3		0.8	V
HIGH-level input current	I_{IH}	V_S=2V	15	30	60	μA
LOW-level input current	I_{IL}	V_S=0.8V	5	15	30	μA

REFERENCE VOLTAGE OUTPUT

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Reference output voltage	Vref	-50μA<I_o<50μA	0.4V_{CC}		0.6V_{CC}	V

(Unless specified otherwise; V_{CC}=5V±5% and -40°C≤T_j≤150°C, typical in V_{CC}=+5V and T_{amb}=25°C).

SUPPLY CURRENT

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Silent	I_{CC}	S=VCC, V_I=VCC		3.6	10	mA
Dominant		V_I=0V, S=0V, LOAD=60Ω		38	70	mA
Recessive		V_I=VCC, S=0V, NO LOAD		3.6	10	mA

(Unless specified otherwise; V_{CC}=5V±5% and -40°C≤T_j≤150°C, typical in V_{CC}=+5V and T_{amb}=25°C).

FUNCTION TABLE

Table1. CAN Transceiver Truth Table

V_{CC}	TXD (1)	S (1)	CANH (1)	CANL (1)	BUS STATE	RXD (1)
4.5V~5.5V	L	L or Open	H	L	Dominate	L
4.5V~5.5V	H or Open	X	$0.5V_{CC}$	$0.5V_{CC}$	Recessive	H
4.5V~5.5V	X	H	$0.5V_{CC}$	$0.5V_{CC}$	Recessive	H
0<V_{CC}<4.5V	X	X	$0V<V_{CANH}<V_{CC}$	$0V<V_{CANL}<V_{CC}$	Recessive	X

(1) H=high level; L=low level; X=irrelevant.

Table2. Driver Function Table

INPUTS		OUTPUTS		Bus State
TXD (1)	S (1)	CANH (1)	CANL (1)	
L	L or Open	H	L	Dominate
H or Open	X	Z	Z	Recessive
X	H	Z	Z	Recessive

(1) H=high level; L=low level; X=irrelevant; Z=high impedance.

Table3. Receiver Function Table

V_{ID}=CANH-CANL	RXD (1)	Bus State (1)
$V_{ID}\geq0.9V$	L	Dominate
$0.5<V_{ID}<0.9V$	?	?
$V_{ID}\leq0.5V$	H	Recessive
Open	H	Recessive

(1) H=high-level; L=low-level; ?=uncertain.

TEST CIRCUIT

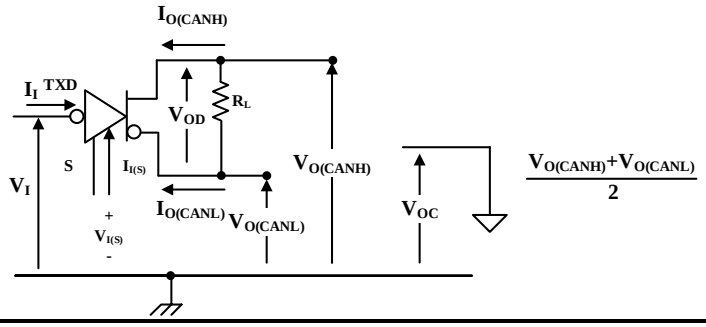


Fig.1 Driver Voltage And Current Definition

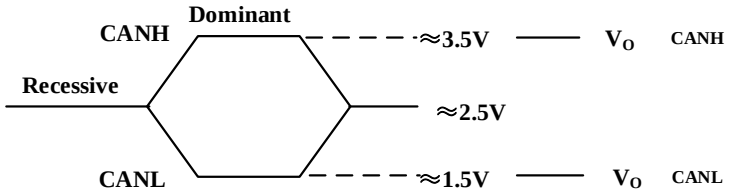


Fig.2 Bus Logic State Voltage Definition

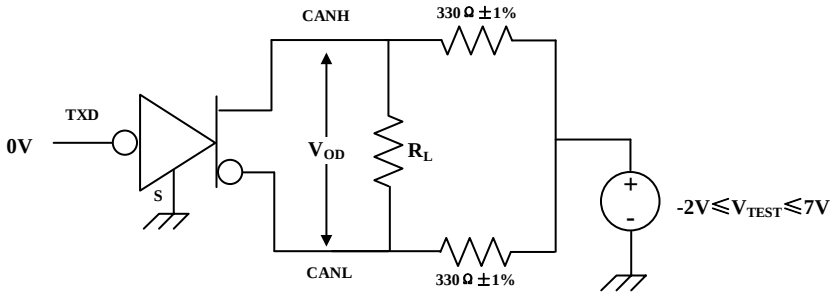


Fig.3 Driver V_{OD} Test Circuit

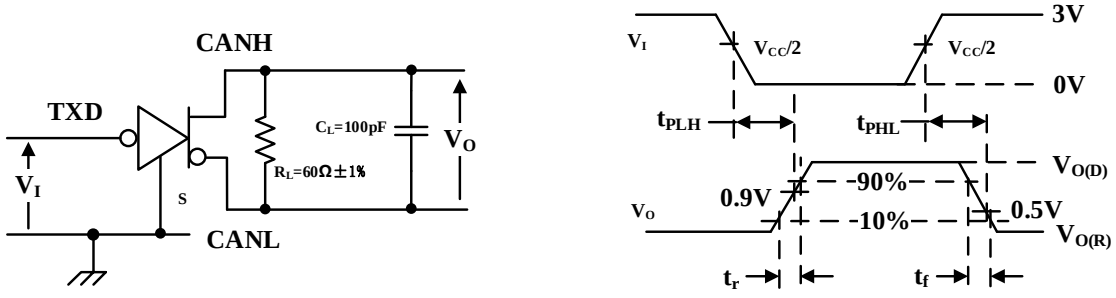


Fig.4 Driver Test Circuit and Waveform

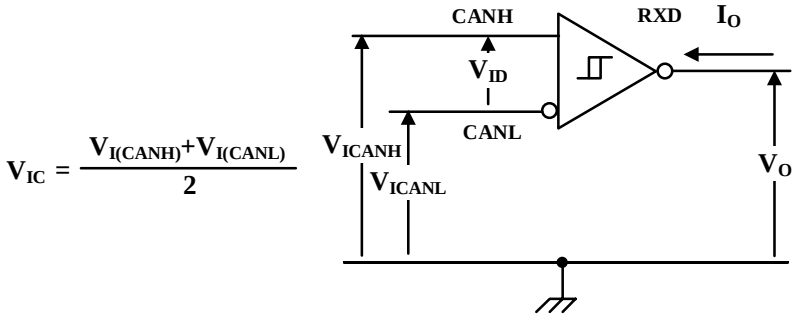
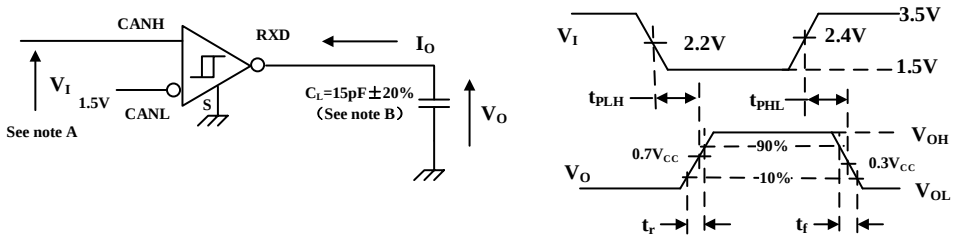


Fig.5 Receiver Voltage and Current Definition



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6ns, Z_O= 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Fig.6 Receiver Test Circuit and Waveform

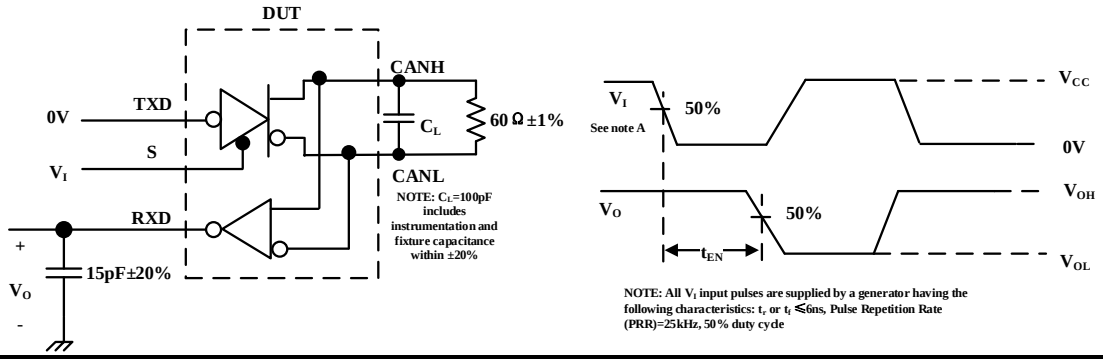
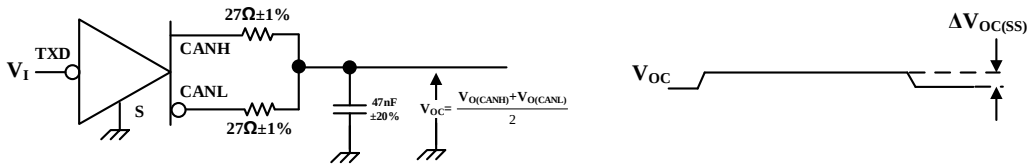


Fig.7 t_{EN} Test Circuit and Waveform



A. All VI input pulses are from 0 V to VCC and supplied by a generator having the following characteristics: tr or tf ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle, ZO = 50 Ω.

Fig.8 Common Mode Output Voltage Test and Waveform

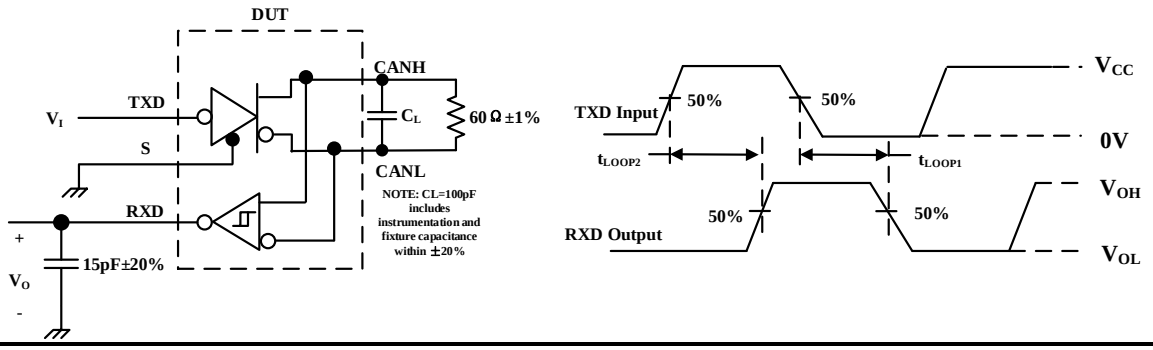
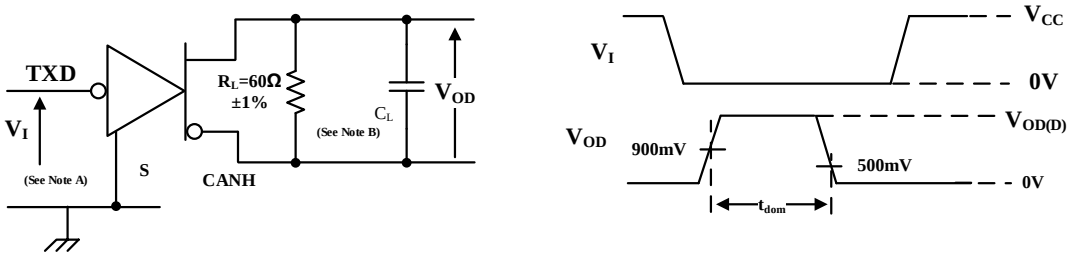


Fig.9 $t_{(LOOP)}$ Test Circuit and Waveform



B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, tr ≤ 6 ns, tf ≤ 6ns, Z_O= 50 Ω.
C. C_L includes instrumentation and fixture capacitance within ±20%.

Fig.10 Dominant Time-Out Test Circuit and Waveform

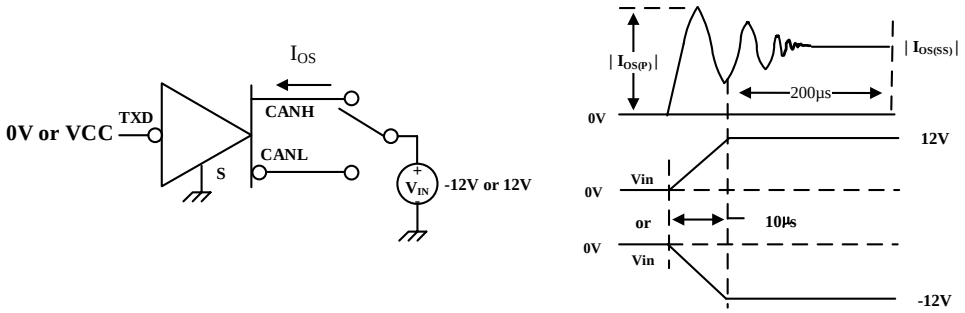


Fig.11 Driver Short-Circuit Current Test Circuit and Waveform

ADDITIONAL DESCRIPTION

1 Sketch

The SIT1050Q is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. It is primarily intended for high-speed applications, up to 1 MBaud, in in-vehicle, industrial control and other fields. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller, and fully compatible with the ISO 11898 standard.

2 Current protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

3 Over temperature protection

SIT1050Q has the function of over temperature protection. After the over temperature protection is triggered, the current of the driving stage will be reduced, because the driving tube is the main energy consuming part. The current reduction can reduce the power consumption and thus reduce the chip temperature. At the same time, other parts of the chip still work normally.

4 TXD dominant time-out function

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{dom}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

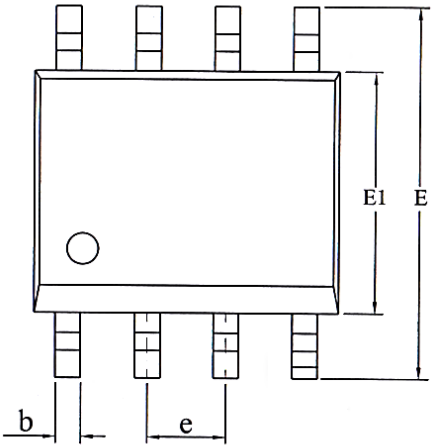
5 Operating modes

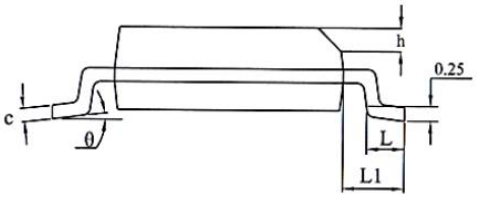
The SIT1050Q provides two modes of operation which are selectable via pin S: High-speed mode and silent mode. The high-speed mode is the normal operating mode and is selected by connecting pin S to ground. Due to an internal pull-down function, it is the default mode if pin S is unconnected. However, to ensure EMI performance in applications using only high-speed mode, it is recommended that pin S be grounded.
In silent mode, the transmitter is disabled. All other IC functions continue to operate. silent mode is selected by connecting pin S to VCC and can be used to prevent network communication blocking due to CAN controller out of control.

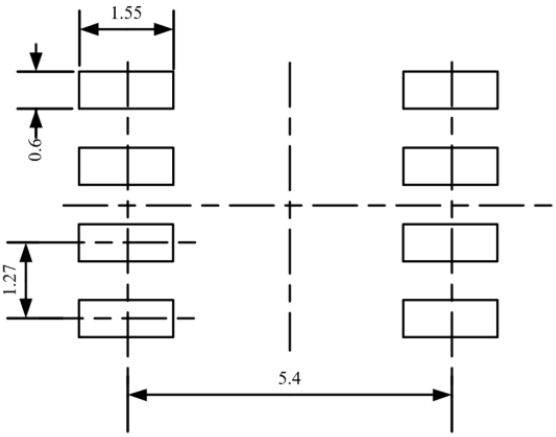
SOP8 DIMENSIONS

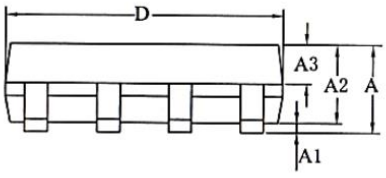
PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.38	-	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.40	0.60	0.80
L1	1.05REF		
c	0.20	-	0.25
θ	0°	-	8°







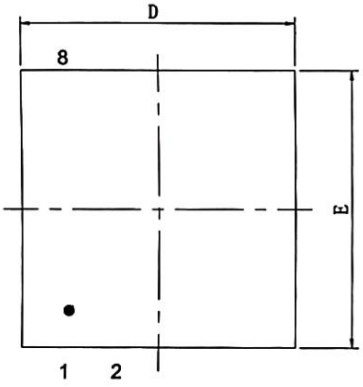


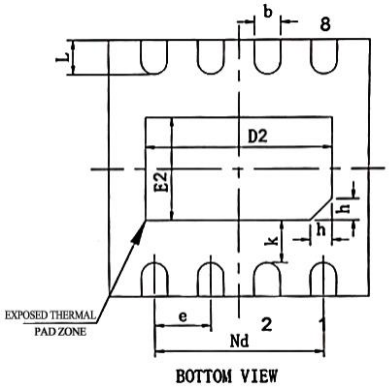
LAND PATTERN EXAMPLE (Unit: mm)

DFN3*3-8 DIMENSIONS

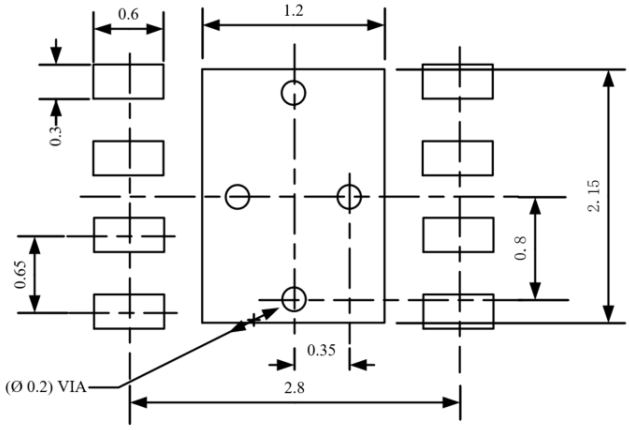
PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.203 REF	
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	2.05	2.15	2.25
Nd		1.95BSC	
E2	1.10	1.20	1.30
b	0.25	0.30	0.35
e		0.65 TYP	
k		0.50REF	
L	0.35	0.4	0.45
h	0.20	0.25	0.30

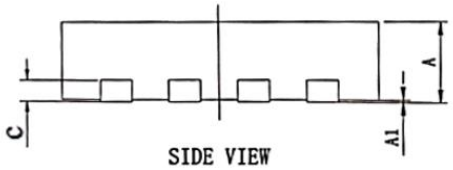




BOTTOM VIEW

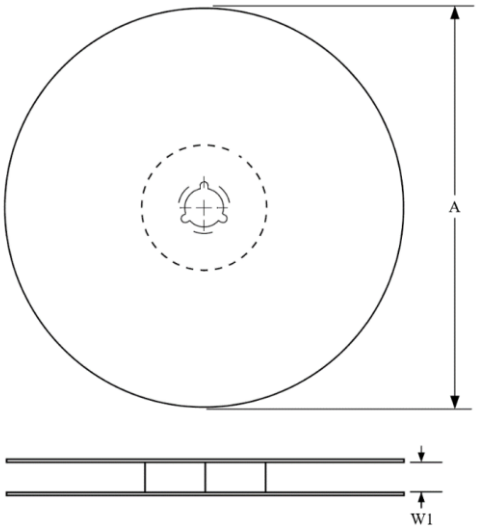


LAND PATTERN EXAMPLE (Unit: mm)

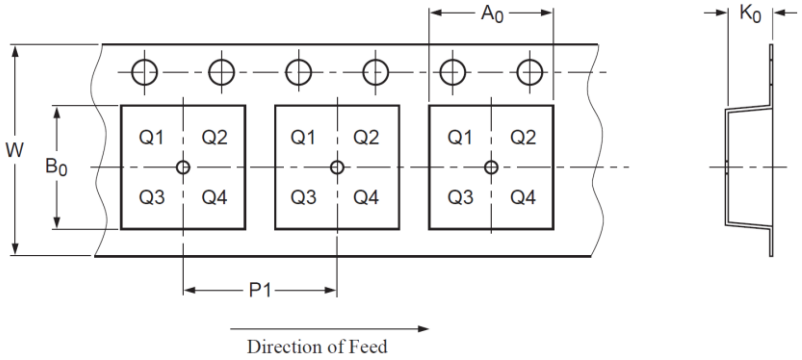


SIDE VIEW

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

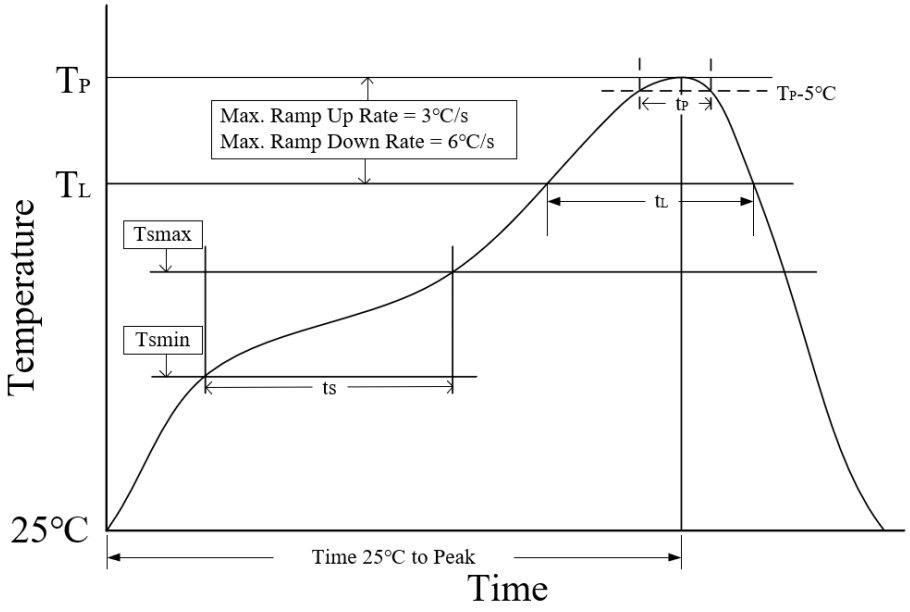
Package Type	Reel Diameter A (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SIT1050QT	SOP8	Tape and reel
SIT1050QTK	DFN3*3-8, small shape, no leads, 8 terminals	Tape and reel

SOP8 package is 2500 pieces/disc. DFN3*3-8 package is 6000 pieces/disc.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature TP time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version	June 2021
V1.1	Deleted CANH, CANL transient voltage parameters; Modified drive propagation delay; Modified CANH, CANL differential input capacitance; Modified CANH, CANL differential input resistance; Added STB pin characteristics; Modified SOP8 package size; Modified DFN3*3-8 package size;	February 2022
V1.2	Modified the range of CANH output voltage (dominant) and CANL output voltage (dominant); Added chip pad information; Added tape information; Added reflow information; Added revision history.	July 2022
V1.3	Added pin configuration diagram of SIT1050QTK; Added ambient temperature T_{amb}; Updated virtual temperature $T_{j;}$ Updated package dimension schematic (size unchanged).	April 2023